

IN THE CLAIMS

Please amend the claims as follows:

Claims 1-5 (Canceled).

Claim 6 (Currently Amended): A signal-processing unit, comprising:

an input ~~line~~ unit configured to provide ~~that is provided with~~ a plurality of analog input signals ~~lines~~;

a multiplexer circuit that ~~transmits~~ receives said plurality of analog signals from said input ~~line~~ unit and outputs the plurality of analog signals to one signal line ~~in a subsequent stage~~ in a desired sequence;

an analog-digital conversion circuit that sequentially converts each ~~an~~ analog signal output from the multiplexer circuit into a digital signal and outputs ~~it~~ the digital signal; and

a cross talk compensation circuit configured (1) to receive ~~that with respect to each of~~ a plurality of the digital signals ~~having been synchronously inputted to a signal-processing unit out of signals having been sequentially outputted from said analog-digital conversion circuit, (2) to assign, for each digital signal of the plurality of digital signals, a corresponding set of coefficients selected so as to compensate for of an interference effect levels between the plurality of analog input signals each of a plurality of signals and the other plural signals interfering with each other is calculated one by one, and (3) to calculate, for each digital signal of the plurality of digital signals, an output value~~ data obtained by multiplying the plurality of digital signals by said corresponding set of coefficients are added up and summing the multiplied signals.

Claim 7 (Currently Amended): The signal-processing unit according to claim 6, wherein ~~[[a]]~~ the cross talk compensation circuit comprises:

a counter that counts ~~the~~ a number of parallel ~~the plurality of digital signals of data~~ input;

a shift register of having a plurality of storage blocks, ~~and that the shift register~~ configured to store said plurality of digital signals and to shift shifts said plurality of digital signals data input to the subsequent stage storage blocks based on a clock period;

a signal hold circuit ~~that holds~~ configured to hold said plurality of digital signals data until ~~all~~ a second plurality of digital signals are stored in said plurality of storage blocks;

a multiplier ~~that multiplies~~ configured to multiply each digital signal of the plurality of digital signals data held in said signal hold circuit by a coefficient of said set of coefficients data having been preliminarily obtained by the calculation of calculating a said signal interference effect levels between the plurality of analog input signals; and

an adder ~~that adds up~~ configured to sum respective the multiplied digital signals of said multiplier and outputs an to output the sum as the output value data of for which cross talk the interference effect level has been compensated.

Claim 8 (Currently Amended): The signal-processing unit according to claim 6, further comprising a communication processing circuit ~~that alters~~ configured to alter a cross talk elimination said set of coefficients to be stored in said cross talk compensation circuit according to input from outside the device communication processing circuit.

Claim 9 (Currently Amended): A signal-processing unit, comprising:

an input ~~line~~ unit configured to provide ~~provided with~~ a plurality of analog input signals lines;

a multiplexer circuit that ~~transmits~~ receives said plurality of analog signals from said input ~~line~~ unit and outputs the plurality of analog signals into one signal line ~~in a subsequent stage~~ in a desired sequence;

an analog-digital conversion circuit that sequentially converts each ~~an~~ analog signal output from the multiplexer circuit into a digital signal and outputs ~~it~~ the digital signal; and

a cross talk compensation circuit configured (1) to receive a ~~that with respect to one~~ digital signal out of the plurality of digital signals ~~having been~~ sequentially outputted from said analog-digital conversion circuit, (2) to assign, for said digital signal, a corresponding set of coefficients selected to compensate for ~~of an~~ interference effect levels between the analog input signal corresponding to the digital signal and the ~~the~~ plurality of analog input signals received before and after said analog input signal and a plurality of signals interfering with each other is calculated, and (3) to obtain output data ~~obtained~~ by multiplying the plurality of digital signals by said corresponding set of coefficients ~~are added up and summing the multiplied signals.~~

Claim 10 (Currently Amended): The signal-processing unit according to claim 9, wherein ~~the~~ the cross talk compensation circuit comprises:

a counter that counts ~~the~~ a number of ~~parallel~~ the plurality of digital signals ~~of data~~ input;

a shift register ~~of~~ having a plurality of storage blocks, ~~and that~~ the shift register configured to store said plurality of digital signals and to shift ~~shifts~~ said plurality of digital signals ~~input to the subsequent stage~~ storage blocks based on a clock period;

a multiplier ~~that multiplies~~ configured to multiply ~~each~~ the digital signal of said plurality of digital signals ~~data~~ held in each of said plurality of storage blocks by a coefficient of said set of coefficients ~~data having been preliminarily obtained by the calculation of~~

calculating ~~[[a]]~~ said signal interference effect levels between the plurality of analog input signals; and

an adder ~~that adds up~~ configured to sum ~~respective~~ the multiplied signals of ~~said~~ multiplier and ~~outputs an~~ to output data the sum as the output data of for which ~~cross-talk~~ the interference effect level has been compensated.

Claim 11 (Currently Amended): The signal-processing unit according to claim 9, further comprising a communication processing circuit ~~that alters~~ configured to alter ~~a cross talk elimination~~ said set of coefficients ~~to be~~ stored in said cross talk compensation circuit according to input from outside the ~~device~~ communication processing circuit.